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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,896	PAWLOWSKI, J. THOMAS	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-63 have been considered but are moot in view of the new ground(s) of rejection.

In regards to applicants argument that none of Curran, Burleson, or de la Iglesia et al teach the newly added claim language of the bus being bidirectional. The above references are all silent as to whether the bus is unidirectional or bidirectional. Therefore the reference to Devanney et al that teaches the claimed bus inversion including an express statement that the bus can be either unidirectional or bidirectional is being applied. Devanney et al only lacks the claimed capturing of the state of a previously transmitted inversion bit.

In regards to applicants argument that de la Iglesia et al does not teach capturing a state of previously transmitted bits: This is incorrect. De la Iglesia et al teaches both Power On Logic Flip (POLF) which captures the previous state and compares it to the present state and Power On Logic State (POLS) which captures the present state and compares it to the total number of bits of data (Column 4 line 66 to Column 5 line 13). The examiner does note that the examiner was unable to find support in the applicants specification that the determining step is based on reducing the number of first bits having a predetermined logic state. Applicants entire specification is directed to reducing the number of transitions (POLF) not the logic state. The examined did find a mention regarding the prior art that, "in some systems, driving a particular binary or logical value on a bit line will consume more power than when the other binary/logical value is driven on the bit line" (POLS). However the examiner was unable to find any indication that the determining from the captured previously transmitted bits whether the first bits should be

inverted was based on reducing the number of first bits having a predetermined state. If you wish to reduce the number of bits having a predetermined state and you are inverting all the bits then you need to know the total number of bits.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim1-13, 17-22, 26-36, 38-49, 51-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Curran PN 5,574,921 in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63: Curran teaches a method of performing bus inversion on first bits (181) to be transmitted on a bus (188), said method comprising the steps of: capturing a state of previously transmitted bits on the bus (186 nbits); capturing a state of an inversion bit associated with the previously transmitted bits (186 sbit); and determining from the captured state of the previously transmitted bits (186 nbits) whether the first bits should be inverted (via 183 184 and 185). Curran is silent upon whether bus 188 is a unidirectional or bidirectional bus. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22). It would have been obvious to use Curran's bit inversion on either a unidirectional or bidirectional bus because this would have prevented limiting the usability of Curran's system.

In regards to claims 2, 27, 49: Curran teaches inverting the bits if it is determined the bits should be inverted (via 185).

In regards to claims 3-4, 9, 21, 28-29, 33: Curran teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 5, 18, 30: Curran teaches inverting if the hamming distance is greater than ½ the number of bits.

In regards to claims 6, 19, 31: Curran teaches taking into account the inversion bit. Curran does not teach computing the hamming distance than taking into account the inversion bit instead Curran teaches taking into account the inversion bit than computing the hamming distance. However in Curran when taking into account the inversion bit, if the hamming distance of the data equal ½ the number of bits than the only bit remaining is the inversion bit. Thus if the value of the inversion bit is 1 than the over all hamming distance will be greater than ½ and the next inversion bit will be set to 1. If the value of the inversion bit is 0 than the over all hamming distance will be less than ½ and the next value of the inversion bit will be set to 0. Thus if the hamming distance of the data is ½ than the next value of the inversion bit will be set to the previous value of the inversion bit. It would have been obvious to a person of ordinary skill in the art at the time of the invention to compute the hamming distance than take into account the inversion bit as a basic principal of math.

In regards to claim 7: Curran teaches the number of bits being N. 50% of all values of N are even.

In regards to claims 8, 20, 32: Curran teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 38-42, 51-54: Curran teaches inverting the "bus" Curran does not limit the type of bus. Curran is silent if the bus is the address, command or data bus. Official Notice is taken that address, data and command buses are well known types of buses. It would have been obvious to a person of ordinary skill in the art at the time of the invention perform Curran's invention on any type of parallel bus because this would have provides for Curran's power savings without limiting the type of bus.

In regards to claim 62: Curran teaches the inversion as described above. Curran only expressly teaches two devices the sending and receiving devices. Curran does not expressly state that there can be more than 2 devices. Official notice is taken that systems with more than 2 devices are common. It would have been obvious to use Curran's bus inversion system in systems.

In regards to claim 10: Curran teaches the number of bits being N. 50% of all values of N are odd.

In regards to claims 11, 34: Curran captures the bits only when bits are available to be transferred.

In regards to claims 12, 35: Curran captures the bits on every transfer.

In regards to claims 13, 22, 36: Curran makes the determination for reducing the number of transitions of the first bits and the inversion bit.

In regards to claims 43-47, 55-60: Curran teaches the number of bits being N. 4,8,9,16 and 32 are included in N.

In regards to claim 61: Curran teaches multiple inversion bits.

4. Claims 1-13, 17-22, 26-36, 38-49, 51-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bus-Invert Coding for low-power I/O by M.R. Stan and W.P. Burleson herein after Burleson in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63: Burleson teaches a method of performing bus inversion on first bits (D0-D7 or sub-buses section III C.) to be transmitted on a bus (bus), said method comprising the steps of: capturing a state of previously transmitted bits on the bus (Pages 53-54 steps 1-4); capturing a state of an inversion bit associated with the previously transmitted bits (invert and description of figure 6)); and determining from the captured state of the previously transmitted bits (D0-D7) whether the first bits should be inverted (steps 1-4). Burleson is silent upon whether the bus is a unidirectional or bidirectional bus. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22). It would have been obvious to use Burleson's bit inversion on either a unidirectional or bidirectional bus because this would have prevented limiting Burleson.

In regards to claims 2, 27, 49: Burleson teaches inverting the bits if it is determined the bits should be inverted (step 2).

In regards to claims 3-4, 9, 21, 28-29, 33: Burleson teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 5, 18, 30: Burleson teaches inverting if the hamming distance is greater than ½.

In regards to claims 6, 19, 31: Burleson teaches taking into account the inversion bit. Burleson does not teach computing the hamming distance than taking into account the inversion bit. However Burleson is silent as to when to take into account the inversion bit, if the hamming distance of the data equal ½ the number of bits than the only bit remaining is the inversion bit. Thus if the value of the inversion bit is 1 than the over all hamming distance will be greater than ½ and the next inversion bit will be set to 1. If the value of the inversion bit is 0 than the over all hamming distance will be less than ½ and the next value of the inversion bit will be set to 0. Thus if the hamming distance of the data is ½ than the next value of the inversion bit will be set to the previous value of the inversion bit. It would have been obvious to a person of ordinary skill in the art at the time of the invention to compute the hamming distance than take into account the inversion bit as a basic principal of math.

In regards to claim 7: Burleson teaches the number of bits being N, in all examples the number of bits being even.

In regards to claim 8, 20, 32: Burleson teaches outputting the inverted/not inverted first bits on the bus; and outputting the inversion bit with a value indicating that the first bits have been inverted/not inverted.

In regards to claims 40, 53: Burleson teaches inverting the data and address buses. Burleson does not limit the type of bus. Official Notice is taken that address, data and command buses are well known types of buses. It would have been obvious to a person of ordinary skill in

the art at the time of the invention perform Burleson's invention on any type of parallel bus because this would have provides for Burleson's power savings without limiting the type of bus.

In regards to claim 62: Burleson teaches the inversion as described above. Burleson does not expressly state that there can be more than 2 devices. Official notice is taken that systems with more than 2 devices are common. It would have been obvious to use Burleson's bus inversion system in systems

In regards to claim 10: Burleson teaches the number of bits being N. 50% of all values of N are odd.

In regards to claims 11, 34: Burleson captures the bits only when bits are available to be transferred.

In regards to claims 12, 35: Burleson captures the bits on every transfer.

In regards to claims 13, 22, 36: Burleson makes the determination for reducing the number of transitions of the first bits and the inversion bit.

In regards to claims 38-39, 51-52: Burleson teaches the bus can also be the address bus.

In regards to claims 41-42, 54: Burleson teaches the bus can be the data bus.

In regards to claims 43-47, 55-60: Burleson teaches the number of bits being N. 4,8,9,16 and 32 are included in N.

In regards to claim 61: Burleson teaches multiple inversion bits.

5. Claims 1, 13-17, 22-26, 36-37, 48, 50, 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over de la Iglesia et al PN 6,490,703 in view of Devanney et al PN 6,243,779.

In regards to claims 1, 17, 26, 48, 63: de la Iglesia et al teaches a method of performing bus inversion on first bits (Fig 2A-2D) to be transmitted on a bus, said method comprising the steps of: capturing a state of previously transmitted bits on the bus (Hamming code); capturing a state of an inversion bit associated with the previously transmitted bits (Flip); and determining from the captured state of the previously transmitted bits whether the first bits should be inverted. de la Iglesia et al is silent upon whether the bus is a unidirectional or bidirectional bus. Devanney et al expressly teaches that bit inversion can either unidirectional or bidirectional (Column 2 lines 21-22). It would have been obvious to use de la Iglesia et al's bit inversion on either a unidirectional or bidirectional bus because this would have prevented limiting the usability of de la Iglesia et al's system.

In regards to claims 13, 22, 36: de la Iglesia et al teaches the determination for reducing the number of transitions of the first bits and the inversion bit (POLF).

In regards to claims 14, 23, 37, 50: de la Iglesia et al teaches the determination for reducing the number of bits having a predetermined logic state (POLS).

In regards to claims 15, 24: de la Iglesia et al teaches the state being a logical 1.

In regards to claims 16, 25: de la Iglesia et al teaches the predetermined logic state being a logical 1. Official Notice is taken that negative logic is well known. It would have been obvious to have the predetermined logic state to be a logical 0 because this would have accounted for systems in which logical 0 consumes more power than logical 1 such as negative logic.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 571 272 3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM
April 26, 2006

PAUL R. MYERS
PRIMARY EXAMINER